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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 2

Complete if Known	
Application Number	09/891,523
Filing Date	June 27, 2001
First Named Inventor	RAKVIC et al
Group Art Unit	2185
Examiner Name	Not assigned
Attorney Docket Number	2207/1123601

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U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

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OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
MI		Agarwal et al, "Column-Associative Caches: A Technique for Reducing the Miss Rate of Direct-Mapped Caches", Proceedings, The 20th Annual Intl Symposium on Computer Architecture, IEEE Computer Society, Technical Committee on Computer Architecture, Association for Computing Machinery SIGARCH, pp 169-190, San Diego, California, May 16-19, 1993	
MI		Alexander et al, "Distributed Prefetch-buffer/Cache Design for High Performance Memory Systems", Proceedings, Second Intl Symposium on High-Performance Computer Architecture, IEEE Computer Society, Technical Committee on Computer Architecture, pp 254-263, San Jose, California, February 3-7, 1996	
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MI		Juan et al, "The Difference-bit Cache", Proceedings, The 23rd Annual Int'l Symposium on Computer Architecture, ACM SIGARCH, IEEE Computer Society, TCCA, pp 114-120, Philadelphia, Pennsylvania, May 22-24, 1996	
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Examiner Signature	Midya Gnoa.	Date Considered	6/2/03

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Unique citation designation number.

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Sheet 2 of 2

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MI		Rau et al, "Pseudo-Randomly Interleaved Memory", Proceedings, The 18th Annual Intl Symposium on Computer Architecture, Association for Computing Machinery, pp 74-83, Toronto, Canada, May 27-30, 1991	
MI		Rivers et al, "On Effective Data Supply for Multi-Issue Processors", Proceedings, Intl Conference on Computer Design, VLSI in Computers and Processors, IEEE Computer Society Technical Committee on Design Automation, IEEE Circuits and Systems Society, pp 519-528, Austin, Texas, Oct. 12-15, 1997	
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MI		Wilson et al, "Designing High Bandwidth On-Chip Caches", "The 24th Annual Intl Symposium on Computer Architecture, Conference Proceedings, ACM, pp 121-132, Denver, Colorado, June 2-4, 1997	
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Examiner Signature	Midya Gnoa	Date Considered	6/2/03